

Serial No. 09/879,724
Attorney Docket No. F0522
Firm Reference No. AMDSP0414US

Reply to Office Action Dated August 19, 2003
Reply Dated September 9, 2003

REMARKS

Claims 1-3, 5 and 17-27 are pending. Claims 20 and 24 are represented including all the features of claims 1 and 18, respectively. Claims 1 and 18 have been amended as suggested by the Examiner. That is, claims 1 and 18 have been amended to include the feature, "wherein the LTCIM layer comprises at least one of doped amorphous silicon having a dopant species selected from one of boron, phosphorous and fluorine, undoped amorphous silicon and undoped porous silicon."

I. ALLOWABLE SUBJECT MATTER

Allowable claims 20 and 24 have been rewritten in independent form including all the limitations of the base claim and any intervening claims. Therefore, claims 20-27 are believed to be in condition for allowance.

II. REJECTION OF CLAIMS UNDER 35 U.S.C. § 102

Claims 1-3, 5 and 17-19 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,285,072 issued to Maeda ("Maeda"). Withdrawal of the rejections is respectfully requested for at least the following reasons.

As illustrated in FIG. 1 of the present specification (reproduced below for the Examiner's convenience) claims 1 and 18 recite a semiconductor-on-insulator (SOI) structure 10. The SOI structure 10 includes a semiconductor substrate 12 (annotation added); a leaky, thermally conductive insulator material (LTCIM) layer 14 (annotation added) disposed directly on the semiconductor substrate 12; and a semiconductor layer 13 (annotation added) disposed directly on the LTCIM layer 14. (See, for example, page 6, lines 8-10).

Additionally, the material of the LTCIM layer 14 includes at least one of doped amorphous silicon, undoped amorphous silicon and undoped porous silicon. Further, when the LTCIM layer 14 is doped amorphous silicon, a dopant species is selected from one of boron, phosphorous and fluorine (annotation added). Further still, the LTCIM layer 14 extends over an

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entire lateral dimension of the semiconductor substrate 12. (See, for example, FIGS. 1-4 and page 6, lines 15-22 and page 7, lines 11-16). Claim 1 further includes active regions defined in the semiconductor layer by isolation trenches and the LTCIM layer (not shown in FIG. 1 below, but see, for example, FIG. 4).

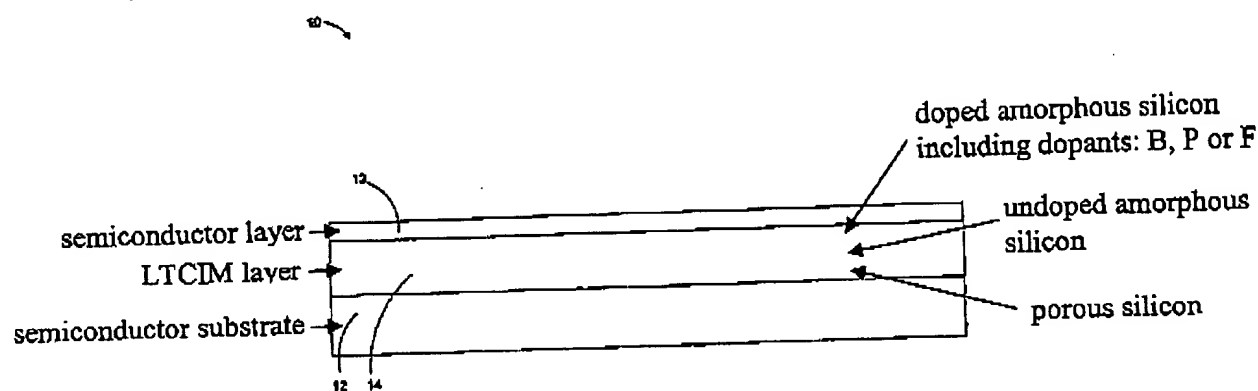


Figure 1: FIG. 1 of Present Specification

Referring now to FIG. 14 of Maeda (also reproduced below for the Examiner's convenience), Maeda discloses a semiconductor device with a silicon region 10 (annotation added) of a first conductivity type. Further, Maeda discloses an active silicon region (annotation added) with a silicon layer 2 including at least one cavity (annotation added) existing inside as a buried layer. Additionally, Maeda discloses a source 17/drain 18 region (annotation added) of a second conductivity type different from the first conductivity type selectively formed on an upper surface of depletion layers 19 and 20, respectively. The depletion layer 19 (annotation added) is formed between the upper surface of the silicon region 10 and the bottom surface of the source 17. The depletion layer 20 (annotation added) is formed between the upper surface of the silicon region 10 and the bottom surface of the drain 18 region. (See, for example, FIG. 14, Col 7, line 64 to Col 8, line 26 and Col 9, line 59 to Col 10, line 13).

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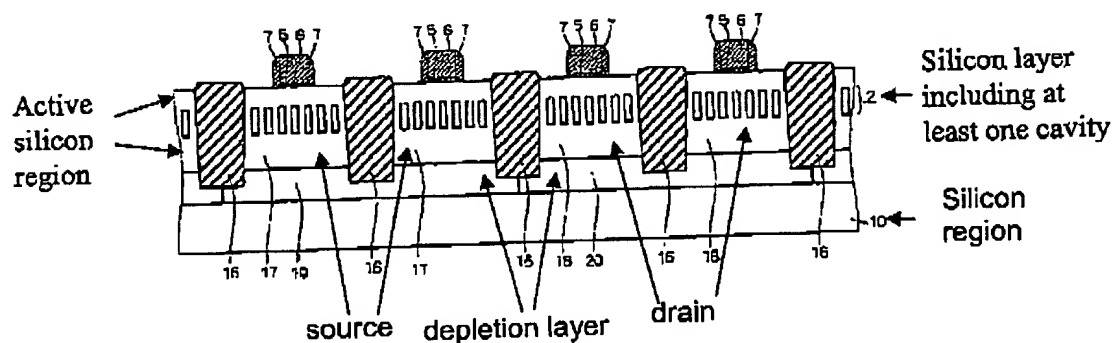


Figure 2: FIG. 14 of Maeda

Maeda does not disclose a leaky, thermally conductive insulator material (LTCIM) layer as claimed in amended claims 1 and 18. That is, Maeda does not disclose the LTCIM to be at least one of doped amorphous silicon having a dopant species selected from one of boron, phosphorous and fluorine, undoped amorphous silicon and undoped porous silicon. Further, Maeda does not disclose the LTCIM layer disposed **directly** on the semiconductor substrate.

Maeda discloses the silicon layer 2 including at least one cavity exists inside the **active silicon region** as a buried layer. Further, the **active silicon region** includes the source 17/drain 18 regions below the silicon layer 2 including at least one cavity. The active silicon region would be the semiconductor layer 13 of the present invention not the LTCIM layer.

Further, the **active silicon region** having the silicon layer 2 including at least one cavity is formed on upper surfaces of the depletion layers 19 and 20. The depletion layers 19 and 20 are formed on the silicon region 10. The depletion layers 19 and 20 are not formed of at least one of doped amorphous silicon having a dopant species selected from one of boron, phosphorous and fluorine, undoped amorphous silicon and undoped porous silicon as claimed in claims 1 and 18. (see, for example, FIGS. 14 and Col 7, line 64 to Col 8, line 26 and Col 9, line 59 to Col 10, line 13)

Therefore, since Maeda does not teach or suggest one or more of the features as claimed in amended claims 1 and 18, claims 1 and 18 and the claims that depend therefrom are patentable over Maeda for at least the reasons stated above.

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III. CONCLUSION

In light of the foregoing, it is respectfully submitted that the present application is in condition for allowance and notice to that effect is hereby requested. If it is determined that the application is not in condition for allowance, the Examiner is invited to initiate a telephone interview with the undersigned attorney to expedite prosecution of the present invention.

Any fee(s) resulting from this communication is hereby authorized to be charged to our Deposit Account No. 18-0988; Our Order No. F0522 (AMDSP0414US).

Respectfully submitted,

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